In the Claims:

Claims 1-5 and 11-15 are canceled. Claims 25-32 are new. The claims are as follows:

1-5. (Canceled)

6. (Currently Amended) A phase lock loop circuit, comprising:

a voltage controlled oscillator adapted to provide a first signal comprising a first frequency;

a phase comparator adapted to compare the first signal comprising the first frequency to a reference signal comprising a reference frequency, the phase comparator being further adapted to provide a control signal representing a phase difference between the first signal and the reference signal; and

a charge pump circuit comprising, a current source, a first field effect transistor (FET), a second field effect transistor (FET), and a first capacitor, wherein the first FET is electrically coupled to the second FET, wherein the first capacitor is electrically coupled to the second FET, wherein the current source is directly connected to a source on the first FET, wherein the current source is coupled between the source on the first FET and ground, wherein the second FET comprises a parasitic capacitance, wherein the charge pump circuit is adapted to receive the control signal and control the voltage controlled oscillator such that a phase of the first signal equals a phase of the reference signal, wherein the second FET is adapted to be operated such that a spark current resulting from a switching mode of the control signal is directed through the parasitic capacitance to ground ~~The phase lock loop circuit of claim 2,~~ and wherein the second

FET is adapted to operate in a saturation mode.

7. (Original) The phase lock loop circuit of claim 6, wherein a direct current (DC) voltage is applied to the gate of the second FET, wherein the DC voltage is less than a minimum voltage value across the first capacitor minus a threshold voltage of the second FET.

8. (Original) The phase lock loop circuit of claim 6, wherein a saturation current value of the second FET is greater that a saturation current value of the current source.

9. (Original) The phase lock loop circuit of claim 6, wherein the second FET comprises a first impedance value between the source and the drain, wherein the parasitic capacitor comprises a second impedance value, and wherein the first impedance value is at least ten times higher than the second impedance value.

10. (Previously presented) The phase lock loop circuit of claim 9, wherein the first impedance value is at least 1 megohm, and wherein the second impedance value is less than or equal to one hundred thousand ohms.

11-15. (Canceled)

16. (Currently Amended) A method, comprising:

providing a phase lock loop circuit comprising a voltage controlled oscillator, a phase comparator, and a charge pump circuit, wherein the charge pump circuit comprises a current source, a first field effect transistor (FET), a second field effect transistor (FET), and a first capacitor, wherein the first FET is electrically coupled to the second FET, wherein the first capacitor is electrically coupled to the second FET, wherein the current source is directly connected to a source on the first FET, wherein the current source is coupled between the source on the first FET and ground, and wherein the second FET comprises a parasitic capacitance;

providing by the voltage controlled oscillator, a first signal comprising a first frequency;

comparing by the phase comparator, the first signal comprising the first frequency to a reference signal comprising a reference frequency;

providing by the phase comparator, a control signal representing a phase difference between the first signal and the reference signal;

receiving by the charge pump circuit, the control signal;

controlling by the charge pump circuit, the voltage controlled oscillator such that a phase of the first signal is about equal to a phase of the reference signal;

discharging by the current source, the first capacitor through the first FET;

operating the second FET such that a spark current resulting from a switching mode of the control signal is directed through the parasitic capacitance to ground, and

~~The method of claim 12, further comprising~~ operating the second FET in a saturation mode.

17. (Original) The method of claim 16, applying a direct current (DC) voltage to the gate of the second FET, wherein the DC voltage is less than a minimum voltage value across the first capacitor minus a threshold voltage of the second FET.

18. (Original) The method of claim 16, wherein a saturation current value of the second FET is greater that a saturation current value of the current source.

19. (Original) The method of claim 16, wherein the second FET comprises a first impedance value between the source and the drain, wherein the parasitic capacitor comprises a second impedance value, and wherein the first impedance value is at least ten times higher than the second impedance value.

20. (Previously presented) The method of claim 19, wherein the first impedance value at least 1 megohm, and wherein the second impedance value is less than or equal to one hundred thousand ohms.

21. (Currently Amended) The phase lock loop circuit of claim [[2]] 6, wherein a frequency of the spark current is at least 10 times higher than a frequency of the current source.

22. (Currently Amended) The phase lock loop circuit of claim 6, wherein a combination of the parasitic ~~capacitor~~ capacitance and the second FET operating in saturation mode form a low pass filter.

23. (Currently Amended) The method of claim [[12]] 16, wherein a frequency of the spark current is at least 10 times higher than a frequency of the current source.

24. (Currently Amended) The method of claim 17, further comprising forming by the parasitic ~~capacitor~~ capacitance and the second FET operating in saturation mode, a low pass filter.

25. (New) The phase lock loop circuit of claim 6, wherein the control signal is applied to the base of the first FET, wherein the first FET is adapted to turn on when the control signal comprises a logical high signal, and wherein the first FET is adapted to turn off when the control signal comprises a logical low signal.

26. (New) The phase lock loop circuit of claim 25, wherein said logical high signal comprises a positive pulse increase signal of the phase lock loop circuit, and wherein said logical low signal comprises a positive pulse decrease signal of the phase lock loop circuit..

27. (New) The phase lock loop circuit of claim 25, wherein the spark current occurs during a transition of the control signal between the logical high signal and the logical low signal.

28. (New) The phase lock loop circuit of claim 6, wherein the first FET is an n-channel FET (NFET), and wherein the second FET is an NFET.

29. (New) The method of claim 16, further comprising applying the control signal to the base of the first FET, wherein the first FET is adapted to turn on when the control signal comprises a logical high signal, and wherein the first FET is adapted to turn off when the control signal comprises a logical low signal.

30. (New) The method of claim 29, wherein said logical high signal comprises a positive pulse increase signal of the phase lock loop circuit, and wherein said logical low signal comprises a positive pulse decrease signal of the phase lock loop circuit.

31. (New) The method of claim 29, further comprising switching between the logical high signal and the logical low signal, wherein the spark current occurs during said switching.

32. (New) The method claim 16, wherein the first FET is an n-channel FET (NFET), and wherein the second FET is an NFET.